Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) The method for predicting performance of an integrated circuit of claim 13 ~~claim 1~~, further comprising a fourth step of predicting the performance of the third circuit from a trend for performances of the first circuit and a circuit of the same type as that of the first circuit and in accordance with a different existing process generation from that of the first circuit,

wherein a predicted value for the performance of the third circuit which has been obtained in the fourth step is used in the third step.

3. (Currently Amended) The method for predicting performance of an integrated circuit of claim 13 ~~claim 1~~, wherein the second step includes a fifth step of predicting a performance correlation coefficient between the third and fourth circuits from a trend for performance correlation coefficients of different existing circuits which are the same types as those of the first and second circuits, respectively, and

the performance correlation coefficient predicted in the fifth step is used in the third step.

4. (Cancelled)

5. (Currently Amended) The method for predicting performance of an integrated circuit of claim 13 ~~claim 1~~, wherein performance of all or part of existing circuits are obtained using simulations, model equations or TCAD (Technology Computer Aided Design).

6. (Currently Amended) The method for predicting performance of an integrated circuit of claim 13 ~~claim 1~~, wherein performance of all or part of existing circuits are obtained using actual measurement.

7. (Currently Amended) A method for designing an integrated circuit, comprising the steps of:

generating a circuit library for a next generation process from prediction results obtained in the method for predicting performance of an integrated circuit of claim 13 ~~claim 1~~; and

performing circuit design based on the generated circuit library using the next generation process.

8-12. (Cancelled)

13. (New) A method for predicting performance of an integrated circuit in an early stage of development, comprising:

a first step of obtaining performance of a first circuit, and obtaining performance of a second circuit which is a different circuit from the first circuit, the first and the second circuits being made by an existing generation process;

a second step of obtaining a performance correlation coefficient between the first circuit and the second circuit; and

using a predicted value or a target value for performance of a third circuit which is the same type as the first circuit and made by a next generation process, and the performance correlation coefficient obtained in the second step, a third step of predicting performance of a fourth circuit which is the same type as the second circuit and made by the next generation process,

wherein at least one of delay time, power consumption and chip area of each of the circuits is used as the performance.